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(54) **SEMICONDUCTOR PACKAGE HAVING WIRE BOND WALL TO REDUCE COUPLING**

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H03F 1/56	(2006.01)
H03F 3/24	(2006.01)
H01L 23/047	(2006.01)
H01L 23/552	(2006.01)
H01L 23/66	(2006.01)
H01L 23/24	(2006.01)

(52) **U.S. Cl.**

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(58) **Field of Classification Search**

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See application file for complete search history.

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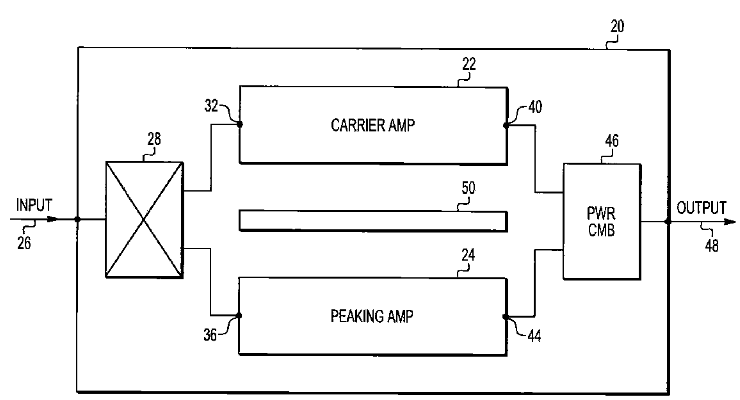
(57) **ABSTRACT**

A system and method for a package including a wire bond wall to reduce coupling is presented. The package includes a substrate, and a first circuit on the substrate. The first circuit includes a first electrical device, a second electrical device, and a first wire bond array interconnecting the first electrical device and the second electrical device. The package includes a second circuit on the substrate adjacent to the first circuit, the second circuit includes a second wire bond array interconnecting a third electrical device and a fourth electrical device. The package includes a wire bond wall including a plurality of wire bonds over the substrate between the first circuit and the second circuit. The wire bond wall is configured to reduce an electromagnetic coupling between the first circuit and the second circuit during an operation of at least one of the first circuit and the second circuit.

26 Claims, 7 Drawing Sheets



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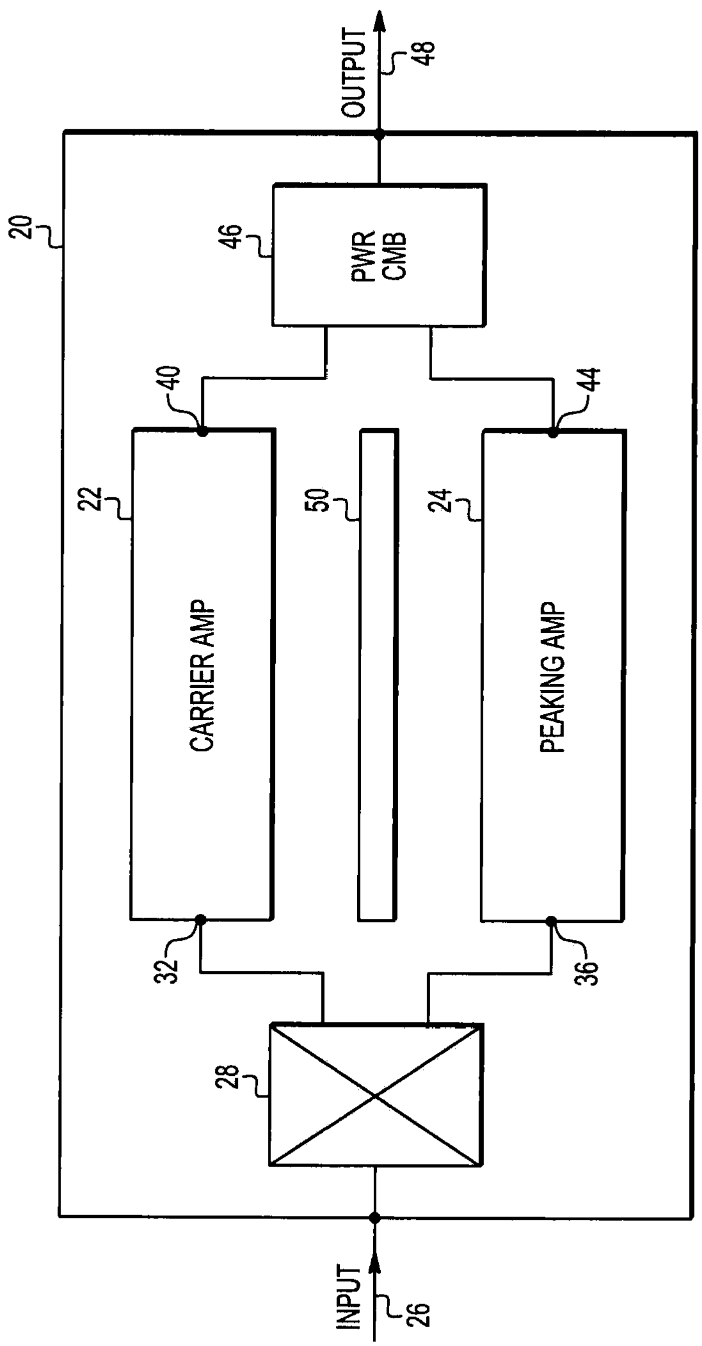
OUTPUT
48
20
46
PWR
CMB
40
44
22
50
24
CARRIER AMP
PEAKING AMP
32
36
28
INPUT
26

FIG. 1

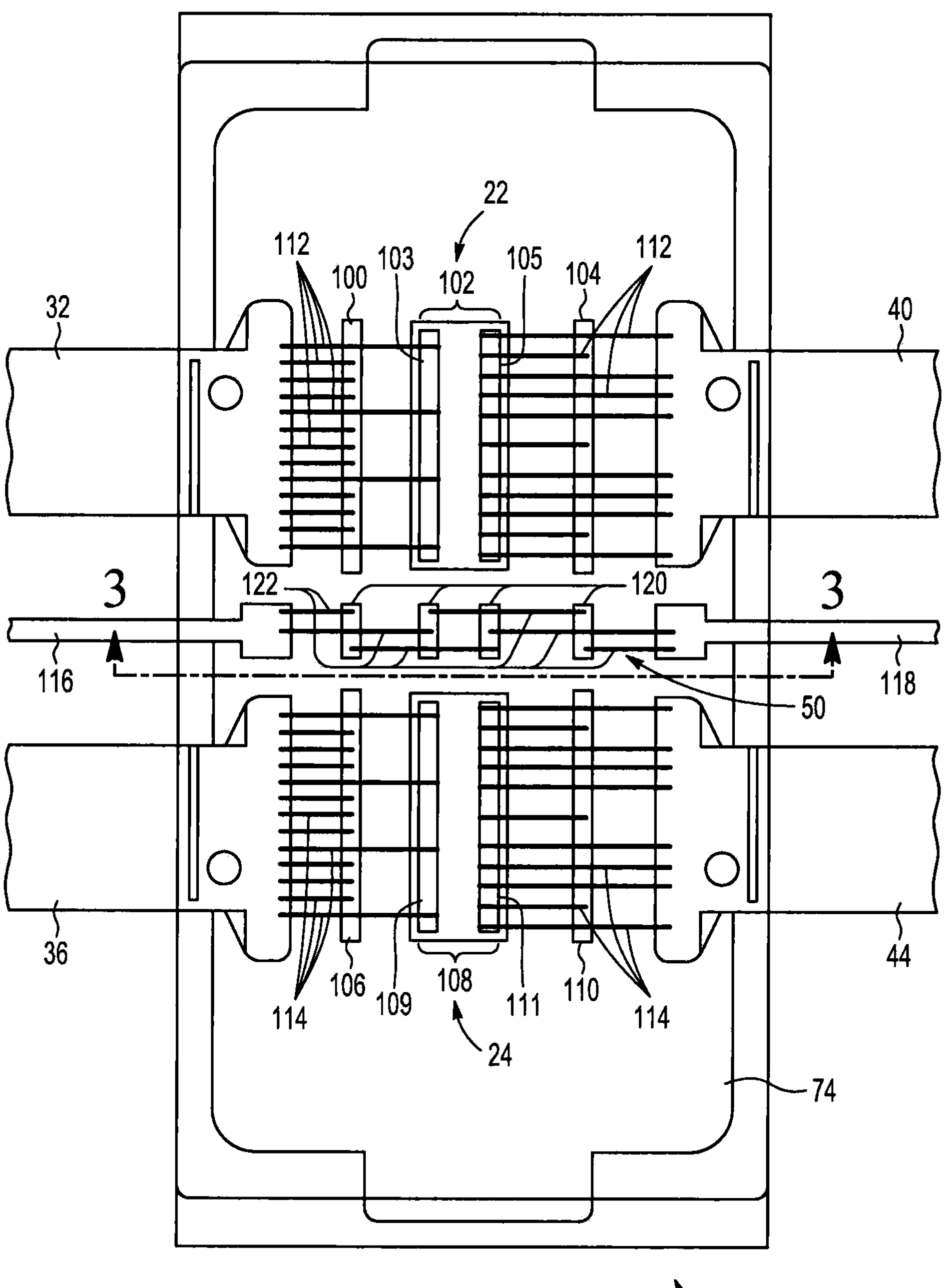
22
112
100
103
102
105
104
112
32
40
3
122
120
3
116
118
50
36
44
106
109
108
111
110
114
114
24
74
20

FIG. 2A

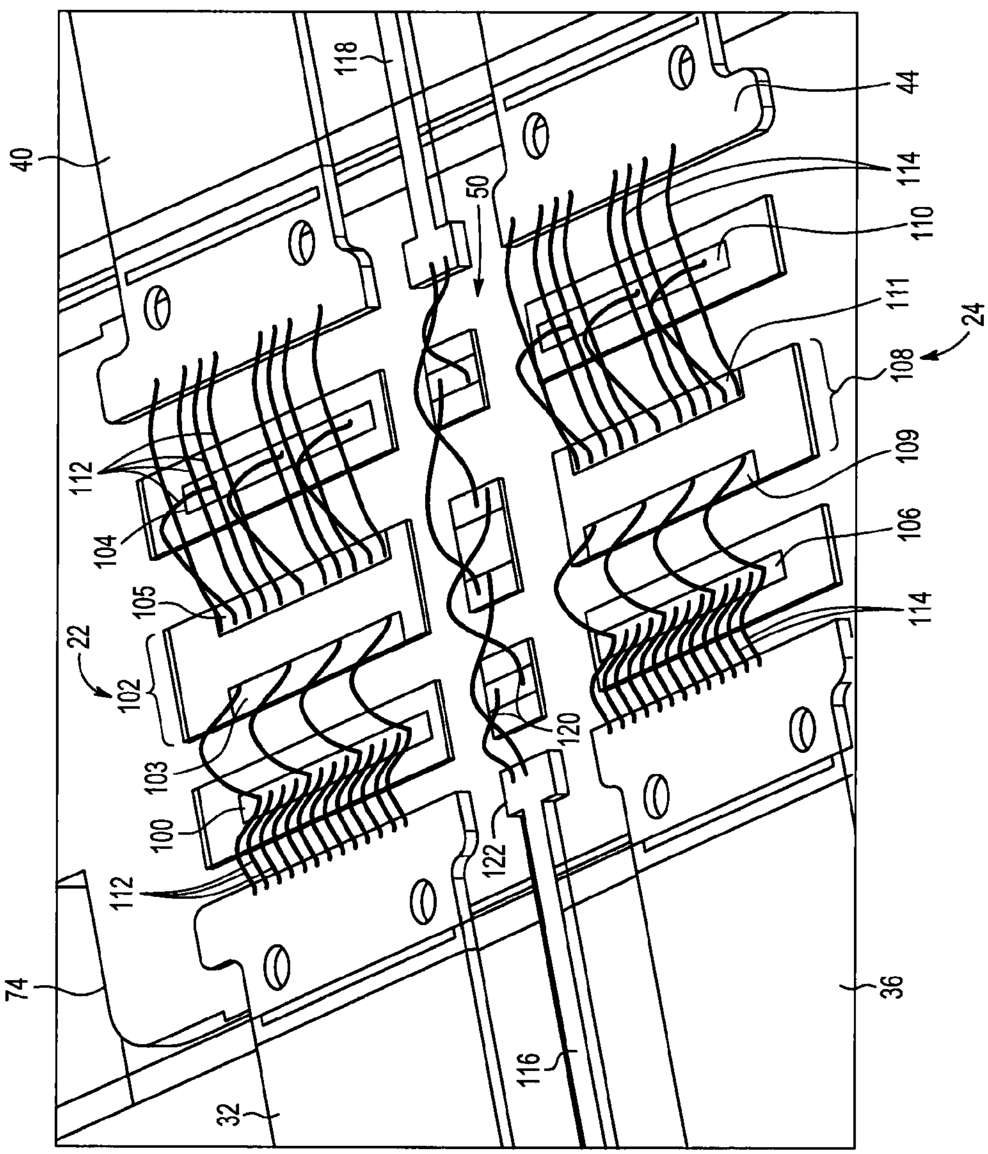
40
118
50
44
114
110
111
24
108
109
106
114
112
104
105
22
102
103
100
120
122
112
74
32
116
36

FIG. 2B

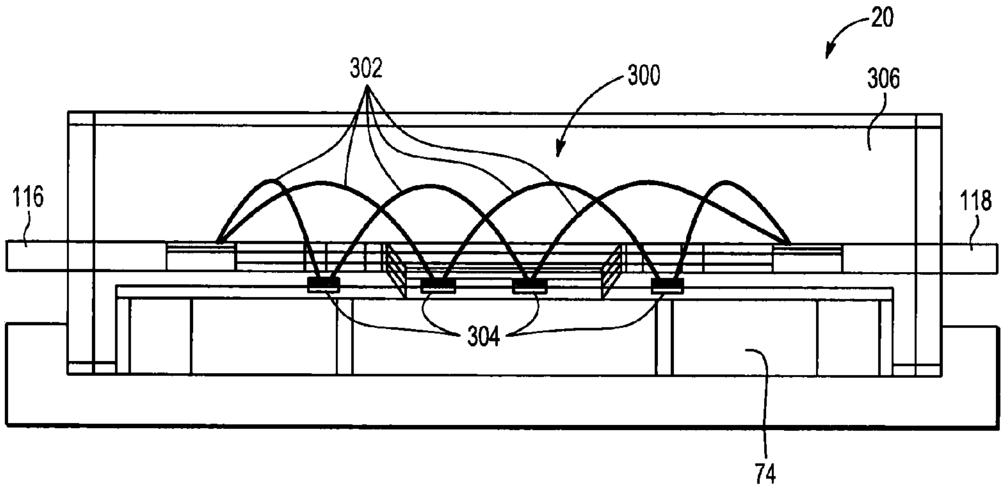

FIG. 3A

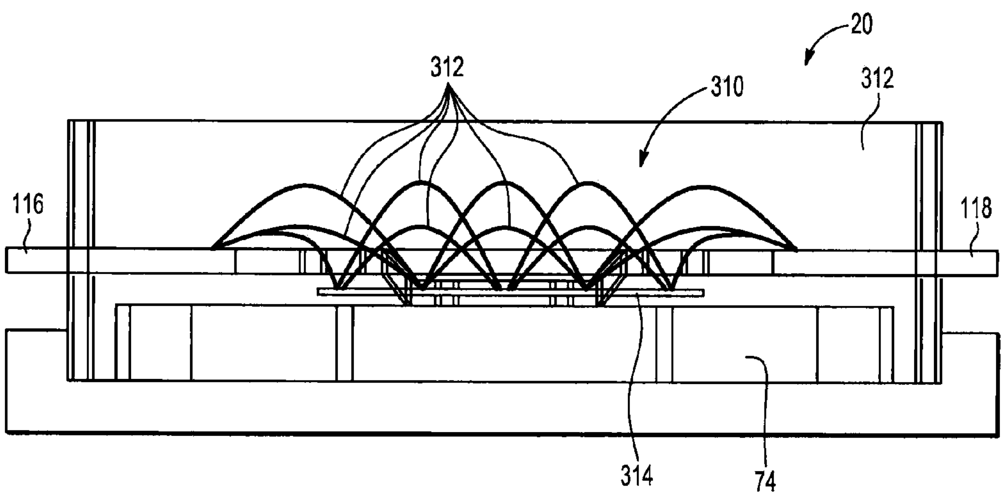

FIG. 3B

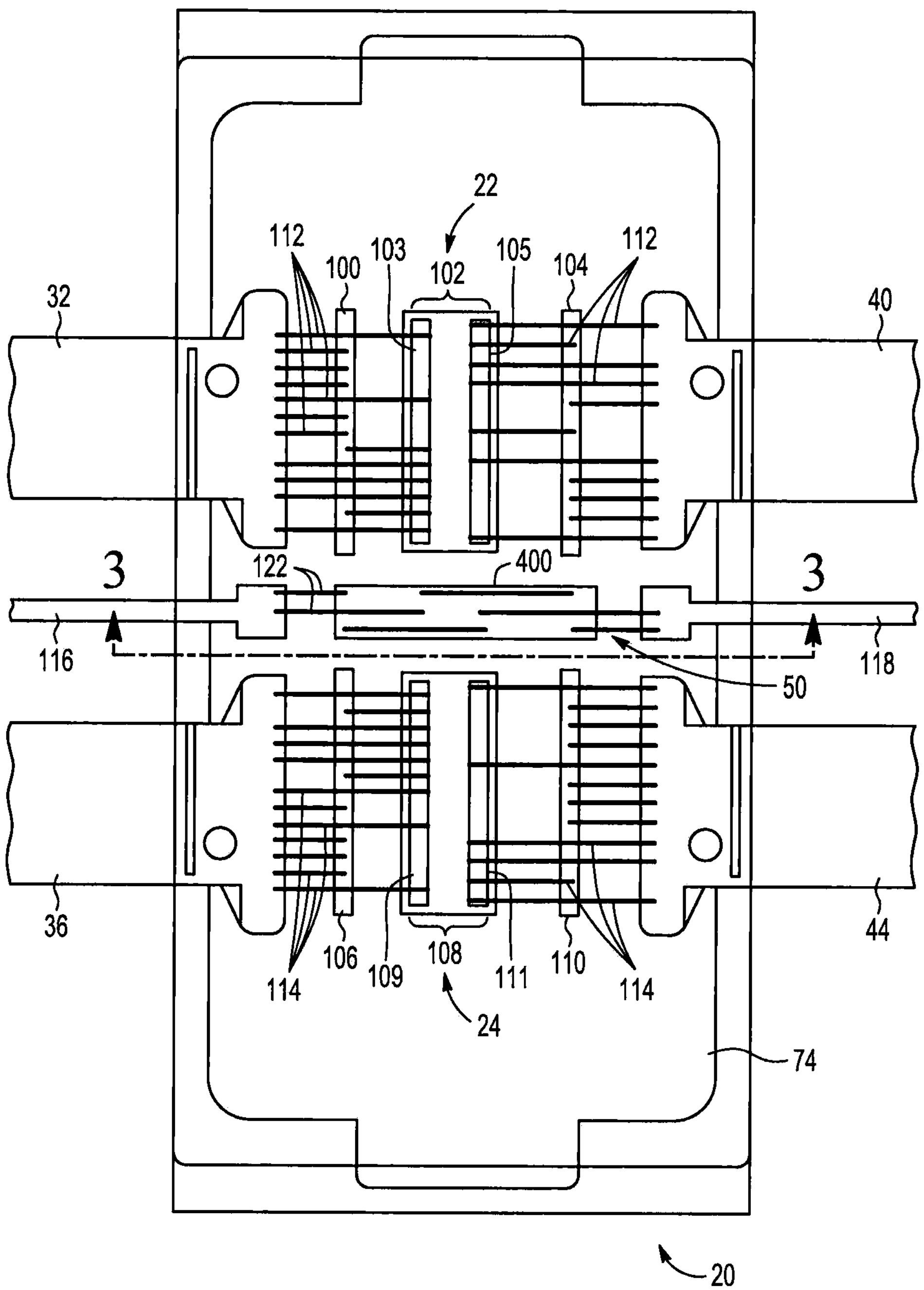
22
112
100
103
102
105
104
112
32
40
3
122
400
3
116
118
50
36
44
114
106
109
108
111
110
114
24
74
20

FIG. 4A

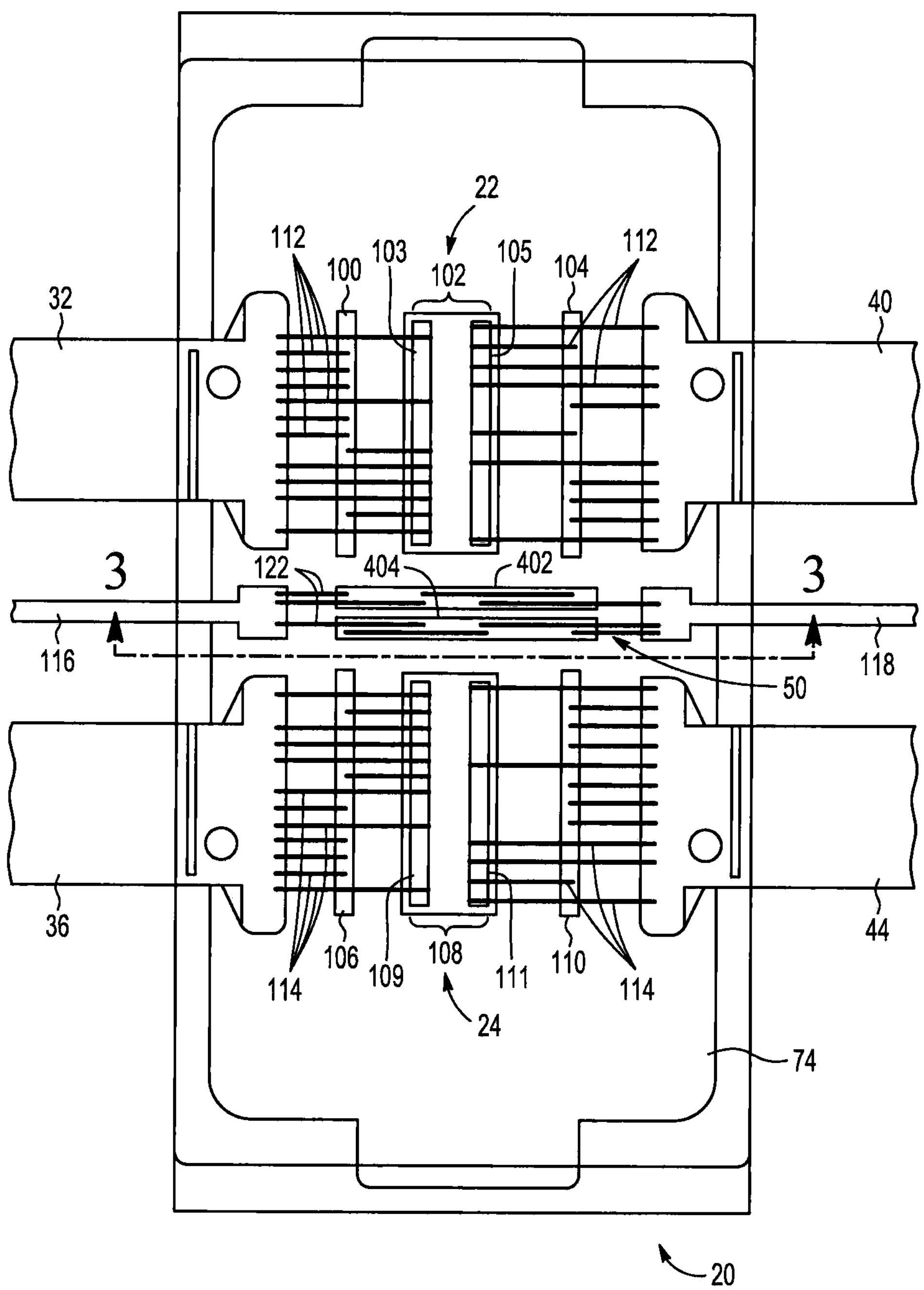
22
112
100
103
102
105
104
112
32
40
3
122
404
402
3
116
118
50
36
44
114
106
109
108
111
110
114
24
74
20

FIG. 4B

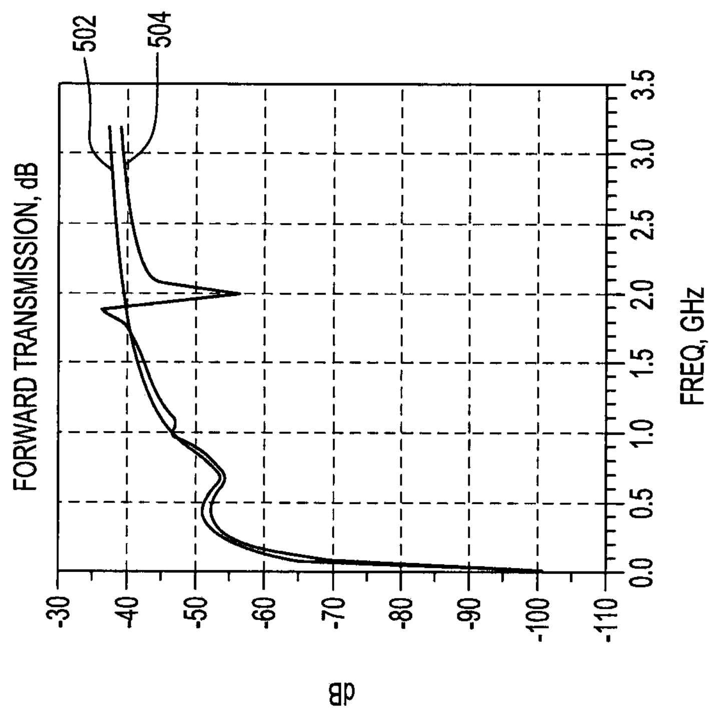
FORWARD TRANSMISSION, dB
502
504
dB
-30
-40
-50
-60
-70
-80
-90
-100
-110
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
FREQ, GHz

FIG. 5A

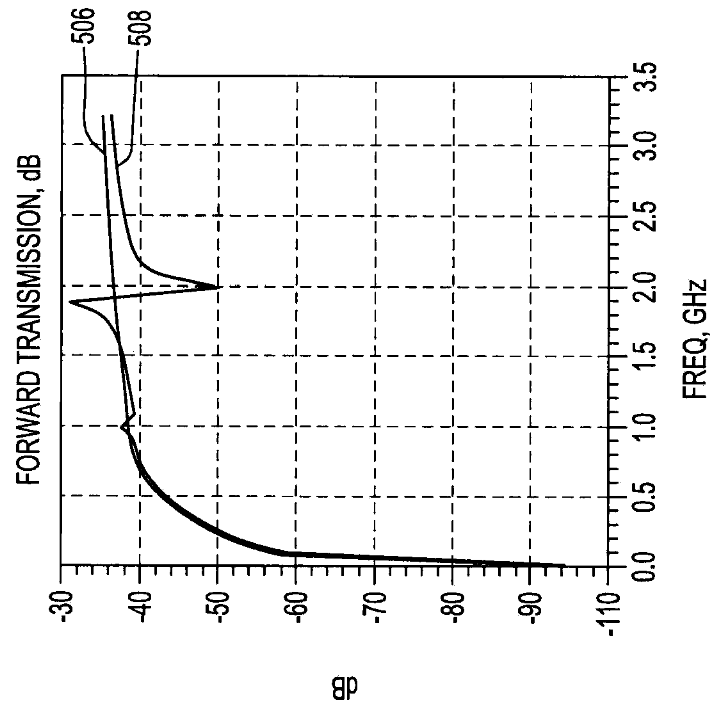
FORWARD TRANSMISSION, dB
506
508
dB
-30
-40
-50
-60
-70
-80
-90
-110
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
FREQ, GHz

FIG. 5B

SEMICONDUCTOR PACKAGE HAVING WIRE BOND WALL TO REDUCE COUPLING

FIELD OF USE

The present disclosure relates generally to device packages, and more specifically, to device packages incorporating a wire bond wall structure to reduce coupling between adjacent devices.

BACKGROUND

Wireless communication systems often employ power amplifiers for increasing the power of a signal. In a wireless communication system, a power amplifier is usually the last amplifier in a transmission chain (the output stage). High gain, high linearity, stability, and a high level of power-added efficiency (i.e., the ratio of the difference between the output power and the input power to DC power) are characteristics of an ideal amplifier.

In general, a power amplifier operates at maximum power efficiency when the power amplifier transmits peak output power. However, power efficiency tends to worsen as output power decreases. Recently, the Doherty power amplifier architecture has been the focus of attention not only for base stations but also for mobile terminals because of the architecture's high power-added efficiency.

A Doherty power amplifier typically includes two or more amplifiers such as a carrier amplifier and a peaking amplifier. These amplifiers are connected in parallel with their outputs joined by an offset transmission line, which performs impedance transformation. The peaking amplifier delivers current as the carrier amplifier saturates, thereby reducing the impedance seen at the output of the carrier amplifier. Thus, the carrier amplifier delivers more current to the load while the carrier amplifier is saturated because of a "load-pulling" effect. Since the carrier amplifier remains close to saturation, a Doherty power amplifier is able to transmit peak output power so that the total efficiency of the system remains relatively high.

The high efficiency of the Doherty architecture makes the architecture desirable for current and next-generation wireless systems. However, the architecture presents challenges in terms of semiconductor package design. Current Doherty power amplifier semiconductor package design calls for the use of discrete devices and integrated circuits that may involve one device that includes the carrier amplifier and a separate device that includes the peaking amplifier. These discrete devices are maintained a distance apart in the package in order to limit problems with crosstalk that can occur between the carrier and peaking amplifiers.

One source of crosstalk in the semiconductor package architecture is between arrays of signal wires, referred to as wire bond arrays, that may be connected between the various electrical devices making up each of the carrier and peaking amplifiers. That is, the performance of a Doherty power amplifier can be adversely affected by coupling (i.e., the transfer of energy from one circuit component to another through a shared magnetic or electric field) between adjacent wire bond arrays of the corresponding components of the Doherty power amplifier. Coupling can be of two types, electric (commonly referred to as capacitive coupling) and magnetic (used synonymously with inductive coupling). Inductive or magnetic coupling occurs when a varying magnetic field exists between current carrying parallel conductors that are in close proximity to one another, thus inducing a voltage across the receiving conductor.

Unfortunately, maintaining spatial distance between amplifiers in the package limits the potential for miniaturization of the semiconductor package. Limiting miniaturization is undesirable where low cost, a low weight, and a small volume are important package attributes for various applications.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is illustrated by way of examples, embodiments and the like and is not limited by the accompanying figures, in which like reference numbers indicate similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. The figures along with the detailed description are incorporated and form part of the specification and serve to further illustrate examples, embodiments and the like, and explain various principles and advantages, in accordance with the present disclosure, where:

FIG. **1** is a block diagram of a Doherty power amplifier semiconductor package.

FIG. **2**A is a top schematic view of the carrier and peaking amplifier circuits of a Doherty power amplifier semiconductor package.

FIG. **2**B is a perspective view of the Doherty power amplifier semiconductor package of FIG. **2**A.

FIGS. **3**A and **3**B are cross-sectional views of a package depicting alternative wire bond wall configurations.

FIGS. **4**A and **4**B show the package of FIG. **2**A where the wire bond wall is connected to a number of additional devices.

FIGS. **5**A and **5**B are graphs showing test results for an example device including a wire bond wall separating a carrier amplifier and peaking amplifier.

DETAILED DESCRIPTION

The following detailed description is exemplary in nature and is not intended to limit the invention or the application and uses of the same. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, or the following detailed description.

For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawings figures are not necessarily drawn to scale. For example, the dimensions of some of the elements or regions in the figures may be exaggerated relative to other elements or regions to help improve understanding of embodiments of the invention.

The terms "first," "second," "third," "fourth" and the like in the description and the claims, if any, may be used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation in sequences other than those illustrated or otherwise described herein. Furthermore, the terms "comprise," "include," "have" and any variations thereof, are intended to cover non-exclusive inclusions, such that a process, method, article, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. The term "coupled," as used herein, is defined as directly or indirectly connected in an electrical or non-electrical manner. As used herein the terms "substantial" and "substantially" mean sufficient to accomplish the stated purpose in a practical manner and that minor imperfections, if any, are not significant for the stated purpose.

The present disclosure relates generally to device packages, and more specifically, to device packages incorporating a wire bond wall to reduce coupling between adjacent devices formed within the package.

In one implementation, the package includes a Doherty amplifier lineup. In the present design, interference and/or cross-talk between the two amplifiers of the Doherty amplifier (i.e., the carrier amplifier and the peaking amplifier) is reduced so that the carrier and peaking amplifiers of the Doherty power amplifier may be implemented in a single package, referred to herein as a dual-path semiconductor package, with improved efficiency. In various other implementations, it will be appreciated that the present system may be used in various packages that include multiple components or circuits that are to be isolated from one another.

The present approach may be used to improve the usability of a Doherty power amplifier semiconductor package in base station power amplifiers, cell phones, blue tooth devices, and other devices dependent upon semiconductor packages, where low cost, low weight, and small volume are desired. An embodiment described herein reduces inductive coupling between wire bond arrays in a Doherty power amplifier. However, it will become apparent that the techniques described below for reducing inductive coupling may be implemented in a variety of semiconductor device designs.

FIG. **1** shows a block diagram of a Doherty power amplifier semiconductor package **20**. Doherty power amplifier semiconductor package **20** includes a carrier amplifier circuit **22** and a peaking amplifier circuit **24** connected in parallel. An input signal **26** is split into two signals by an input splitter **28**. One of the resulting input signals is communicated to an input **32** of carrier amplifier circuit **22**, and another input signal is communicated to an input **36** of peaking amplifier circuit **24**. An output signal is communicated from an output **40** of carrier amplifier circuit **22**. Likewise, an output signal is communicated from an output **44** of peaking amplifier circuit **24**. The two output signals are combined through a power combiner (PWR CMB) **46** to produce a combined output signal **48**. Those skilled in the art will recognize that a Doherty power amplifier semiconductor package typically includes additional electronic devices and circuitry not shown herein for simplicity of illustration.

In one embodiment, carrier amplifier circuit **22** is configured to be on for an entire range of output powers of Doherty power amplifier semiconductor package **20**. Peaking amplifier circuit **24** is configured to turn on only when carrier amplifier circuit **22** saturates. Power combiner **46**, operating to combine the output signal from carrier amplifier circuit **22** with the output signal from peaking amplifier circuit **24** may be a quarter-wave impedance inverter. The quarter-wave impedance inverter can add a ninety degree lag to the output signal from carrier amplifier circuit **22**. The phase of peaking amplifier circuit **24** is typically designed to lag carrier amplifier circuit **22** by ninety degrees so that the two output signals add in-phase when the output signals are combined at the output of power combiner **46** to form combined output signal **48**.

In the example shown in FIG. **1**, each of carrier amplifier circuit **22** and peaking amplifier circuit **24** may include a number of active and passive electrical elements. For example, carrier amplifier circuit **22** may include a capacitor coupled to input **32**. The capacitor can be coupled to a transistor, which applies the appropriate amplification to the input signal received at input **32**. An output of the transistor can be connected to a second capacitor. The capacitors can operate to condition the input signal received at input **32** and amplified by the transistor. Similarly, peaking amplifier **24** can include a capacitor coupled to input **36**. The capacitor can be coupled to a transistor, which applies the appropriate amplification to the input signal received at input **36**. An output of the transistor can be connected to a second capacitor. The capacitors can operate to condition the input signal received at input **36** and amplified by the transistor. Those skilled in the art will recognize that carrier amplifier circuit **22** and peaking amplifier circuit **24** may include additional electronic devices not shown herein for simplicity of illustration.

In Doherty amplifier package **20**, the separate electrical devices making up each of carrier amplifier **22** and peaking amplifier **24** may be connected to one another using multiple parallel wires, known as wire bonds. In a practical application, one or more of the signal paths (e.g., between inputs, outputs, capacitors and transistors thereof) of carrier amplifier circuit **22** may be established using wire bonds. Likewise, one or more of the signal paths (e.g., between inputs, outputs, capacitors and transistors thereof) of peaking amplifier circuit **24** may be established using wire bonds.

In a Doherty power amplifier package, these various wire bond arrays may be placed in very close proximity to one another due to their being packaged into a single housing. The small distances between the signal paths of the various wire bonds interconnecting the components of each amplifier can lead to relatively high levels of inductive coupling between adjacent wire bond arrays. This inductive coupling can limit the power capability of an in-package Doherty amplifier.

Accordingly, in the present Doherty amplifier package, wire bond wall **50** is formed between the two amplifiers **22** and **24** to provide electrical isolation between the wire bonds arrays of each amplifier (e.g., carrier amplifier **22** and peaking amplifier **24**). Wire bond wall **50**, as described further below, is constructed from a number of wire bond connections formed within the package between the circuitry making up the carrier and peaking amplifiers. Wire bond wall **50**, depending upon the implementation of package **20**, may be built on various substrates or directly upon a leadframe of package **20**. Along with the other components of package **20**, wire bond wall **50** may be over molded with encapsulant or may be part of an air cavity package. In various implementations, wire bond wall **50** may be connected directly to ground or to a ground terminal which may, in turn be connected to a ground voltage, or connected to various integrated passive devices (IPDs) or other active devices and circuitry. In general, wire bond wall **50** operates as a shield or fence to interrupt and prevent the inductive coupling between the carrier amplifier circuit and the peaking amplifier circuit of the Doherty amplifier.

FIG. **2**A is a top schematic view of carrier amplifier **22** circuit and peaking amplifier **24** circuit of Doherty power amplifier semiconductor package **20**. FIG. **2**B is a perspective view of Doherty power amplifier semiconductor package **20** of FIG. **2**A. Although the present example is explained in terms of components of a Doherty amplifier, it should be understood that the present system and method may be employed to provide electrical isolation for any circuits formed over a substrate, where the components of a Doherty amplifier are only one example. In accordance with the present disclosure, a wire bond wall may be utilized to provide for electrical isolation between any components, suitably configured, within a particular package. For example, with reference to FIGS. 2A and 2B, carrier amplifier **22** may be replaced by any electrical circuit including a number of interconnected electrical devices and peaking amplifier **24** may be similarly replaced.

In package **20**, carrier amplifier **22** includes input terminal **32** and output terminal **40**, which, in a Doherty configuration, may constitute a gate terminal and a drain terminal of carrier amplifier **22**, respectively. Similarly, peaking amplifier **24** includes input terminal **36** and output terminal **44**, which, in a Doherty configuration, may constitute a gate terminal and a drain terminal of peaking amplifier **24**, respectively.

Carrier amplifier **22** includes a number of electronic devices, such as capacitors **100** and **104** and transistor **102** (having gate pad **103** and drain pad **105**) manufactured and/or subsequently mounted to the surface of a common (i.e., single) carrier, such as a package ground plane **74**. Capacitors **100** and **104** may be, for example, Metal-Oxide-Semiconductor (MOS) capacitors mounted on ground plane **74**. Similarly, peaking amplifier **24** includes a number of electrical devices, such as capacitors **106** and **110** and transistor **108** (having gate pad **109** and drain pad **111**) manufactured and/or subsequently mounted to the surface of a common (i.e., single) carrier, such as a package ground plane **74**. Capacitors **106** and **110** may be, for example, Metal-Oxide-Semiconductor (MOS) capacitors mounted on ground plane **74**.

As shown in FIGS. 2A and 2B, the components of carrier amplifier **22** (including capacitors **100** and **104**, transistor **102**, and terminals **32** and **40**) are connected by a number of wire bonds **112** forming an array of wire bonds. The components of peaking amplifier **24** (including capacitors **106** and **110**, transistor **108**, terminals **36** and **44**) are similarly connected by a number of wire bonds **114**, themselves forming an array of wire bonds. In various implementations, any number of wire bonds may be used to interconnect the various components of carrier amplifier **22** and peaking amplifier **24**, or any other components that may be formed over a surface of ground plane **74**.

In the depicted package **20**, the symmetrical layout of carrier and peaking amplifier circuits **22** and **24** can result in the corresponding components of carrier amplifier circuit **22** being adjacent to corresponding components of peaking amplifier circuit **24**. Accordingly, the arrangement of various components of each amplifier (including, specifically, the wire bonds **112** and **114** of each amplifier carrying high-frequency signals) are adjacent to and geometrically parallel with one another. These attributes of the wire bond arrays of carrier amplifier **22** and peaking amplifier **24** can result in coupling between the devices, which can reduce the performance of the overall device.

To minimize coupling between carrier amplifier **22** and peaking amplifier **24**, package **20** includes wire bond wall **50** separating carrier amplifier **22** and peaking amplifier **24**. Wire bond wall includes terminals **116** and **118** which, in one implementation, can each be connected to ground. A number of connection pads **120** are formed over a surface of ground plane **74**. In one implementation, each of connection pads **120** are connected to a ground voltage, for example, by connecting the connection pads **120** to a ground plane (e.g., ground plane **74**) of package **20** or to one or more ground terminals that can then be connected to a ground voltage. A number of wire bonds **122** are then formed between the connection pads **120** and terminals **116** and **118**. The position and geometrical configuration of connection pads **120** enables the various wire bonds **122** making up wire bond wall **50** to be separated by an appropriate pitch distance, depending upon the implementation of package **20**. In one implementation, the pitch distance is between 5 and 6 millimeters (mm).

As a whole, wire bonds **122** form a wall or mesh of grounded wire bonds that operate to electrically isolate carrier amplifier **22** from peaking amplifier **24**. Wire bonds **122** may be formed of a suitable conductive metal the same as or different from that of wire bonds **112** and/or **114**. Example materials include gold, copper, aluminum, or silver. In one implementation, wire bond wall **50** and wire bonds **122** thereof operate as a passive device configured to absorb and, thereby, block or inhibit the electric fields generated by carrier amplifier **22** and peaking amplifier **24** from impinging upon one another. Depending upon the implementation, the configurations of wire bonds **122** may be adjusted or tuned to serve particular needs, such as to block particular frequency ranges or particular bandwidths. These adjustments may involve changing the lengths of the individual wire bonds **122** that make up wire bond wall **50** and the degree to which the various wire bonds overlap one another. Once formed, an encapsulant (not shown) may be deposited over package **20** to provide physical protection to the wire bonds therefore, as well as the other components of package **20**.

In various implementations, wire bond wall **50** includes a number of wire bonds that are formed along a route between two circuits or components that are to be isolated from one another. When wire bond wall **50** runs along a straight line, the wire bonds **122** making up wire bond wall **50** are each formed generally parallel to one another. As shown in FIG. 2B, wire bond wall **50** may run along a route or pathway that is perpendicular to a line drawn between carrier amplifier **22** and peaking amplifier **24**. Generally, wire bond wall **50** runs along a region of ground plane **74** that is located between carrier amplifier **22** and peaking amplifier **24**. Within wire bond wall **50**, the individual wire bonds **122** may be formed in a single row, or, as depicted in FIG. 2A, multiple rows. FIG. 2A shows wire bond wall **50** including three rows of wire bonds **122**. Also, as depicted in FIG. 2B, the wire bonds **122** making up wire bond wall **50** can connect to every connection pad **120** of wire bond wall **50** or may, in some cases, skip over connection pads **120**.

When a wire bond wall is made up of multiple rows of wire bonds, one approach for constructing the wire bond wall is to provide that, for each connection pad, at least one wire bond from one row of the wire bond wall is connected to the connection pad and at least one wire bond from another row is not connected to the connection pad. This approach can provide that the wire bonds making up the wire bond wall form a mesh that, when viewed from the side, has smaller openings than if the wire bonds of each row were to be identically connected.

In addition to running along a straight line, the wire bond wall may be formed along non-straight routes. In some cases, non-straight routes may be called for by the layout and/or geometry of the circuitry being isolated. In other implementations, the wire bond wall may be formed substantially around a particular circuit. This may enable a circuit in the package to be isolated not only from other circuits in the package, but from radiation sources external to the package.

To illustrate some different configurations of wire bond wall **50**, FIGS. **3**A and **3**B are cross-section views of a package depicting alternative wire bond wall configurations. The cross-section could be taken, for example, along line **3-3** shown in FIG. **2**A, but illustrate different wire bond wall configurations than that shown in FIG. **2**A. In FIG. **3**A, wire bond wall **300** is formed by a number of wire bonds **302** interconnecting connection pads **304** and terminals **116** and **118**. A protective encapsulant **306** is formed over wire bonds **302**. In FIG. **3**B wire bond wall **310** is formed by a number of wire bonds **312** over a ground plane or connection pad structure **314** and interconnecting terminals **116** and **118**. A protective encapsulant **316** is formed over wire bonds **312**. The configuration illustrated in FIG. **3**B includes a greater number of wire bonds compared to that of FIG. **3**A and, as such, the wire bond wall of FIG. **3**B, when viewed from the side, has greater density, reducing the average size of the openings in wire bond wall **50**.

Generally, the configuration of wire bond wall **50** is selected to absorb and thereby block electromagnetic transmissions in a particular range of frequencies. In many cases, the frequencies being blocked are the operating frequencies of the devices formed within the package. For a given implementation, a number of candidate wire bond walls configurations may be simulated where the various candidates include varying numbers of wire bonds, varying lengths of wire bonds, varying numbers of rows of wire bonds, and a different number of overlapping wire bonds to determine their responses to particular input signals. One example tool for performing such simulations includes HFSS, which is a tool useful for antenna design. Then, in accordance with the desired circuit performance, a particular wire bond wall design can be selected.

In FIGS. **2**A and **2**B, wire bond wall **50** may be grounded or floating and generally operates as a passive component of package **20**. In essence, when grounded, wire bond wall **50** operates as a tuned antenna configured to absorb the electromagnetic emissions of either of carrier amplifier **22** and peaking amplifier **24** to prevent those emissions from impinging upon the other circuit.

In some implementations, wire bond wall **50** may be connected to one or more passive or active devices to further control and/or optimize the response of wire bond wall **50**. The additional devices may be formed within package **20**, or may be external to package **20**. To illustrate, FIGS. **4**A and **4**B show package **20** where wire bond wall **50** is connected to a number of additional devices. As shown in FIG. **4**A, wire bond wall **50** is connected to IPD **400**. IPD **400** may include combinations of resistors, capacitors, and inductors that are formed within package **20**. Generally, a capacitance and/or inductance of IPD **400** will be selected so that, when connected to wire bond wall **50**, the impedance of wire bond wall **50** in combination with IPD **400** is tuned to block a desired range of signal frequencies. This impedance matching serves to minimize the coupling between carrier amplifier **22** and peaking amplifier **24**, thereby improving the efficiency of the package **20**. By tuning the performance of the wire bond wall **50** by incorporating IPD **400**, a reduction in coupling can be achieved over a particular frequency range. FIG. **4**B illustrates an alternative embodiment including two IPDs **402** and **404**, where IPDs **402** and **404** run parallel to one another. IPDs **402** and **404** are coupled to wire bond wall **50**. In various implementations, any number of IPDs may be provided in combination with wire bond wall **50** to provide electrical isolation of the components of package **20**.

In other implementations, wire bond wall **50** may also be connected to one or more active devices that may be configured to modify an impedance of wire bond wall **50** depending upon the operational attributes of carrier amplifier **22** and peaking amplifier **24** (or other circuits of package **20**) or other system components. In that case, the active devices may be tunable depending upon a particular operating frequency of the circuits of package **20**, for example, to meet particular frequency and/or bandwidth requirements.

In addition to providing the electrical isolation benefits described above, the present wire bond wall implementation is additionally beneficial in that it may be constructed using similar fabrication techniques that are used to manufacture the remainder of package **20**. The wire bonds of the wire bond wall can, in some implementations, be fabricated using the same wire bonding techniques used to interconnect the components of carrier amplifier **22** and peaking amplifier **24**, for example. This stands in contrast to some other isolation techniques that may require a radical redesign of the structure of package **20**. For example, if a solid metal wall were to be disposed between carrier amplifier **22** and peaking amplifier **24** in an attempt to provide electrical isolation, entirely new fabrication techniques (and, potentially, machinery) would have be developed and utilized to install such a structure within an existing package design. In fact, in many cases, the packages would have to be entirely redesigned to incorporate such a component.

In simulation, embodiments of the present wire bond wall structure have demonstrated improved performance over a conventional package. In one simulation of a Doherty structure including a wire bond wall configured in accordance with the depiction in FIG. **3**B operating at approximately 2 GHz, a grounded wire bond wall reduced detected coupling by approximately 3 dB and a wire bond wall with integrated IPD reduced detected coupling by approximately 17 dB. For comparison, a reduction of only 5 dB was observed in simulations when a solid metal wall was positioned between the components of the Doherty amplifier.

FIGS. **5**A and **5**B are graphs showing simulation results for an example device including a wire bond wall configured in accordance with the depiction of FIG. **3**B separating a carrier amplifier and peaking amplifier within a single package, where the wire bond wall is connected to a suitably configured IPD. The graphs depict an amount of coupling between nodes within the package (vertical axis, dB) versus frequency (horizontal axis, GHz). FIG. **5**A depicts the test results as measured between elements **105** and **44** of FIG. **2**A. FIG. **5**B depicts the test results as measured between elements **40** and **44** of FIG. **2**A.

In FIG. **5**A, line **502** shows the results for a conventional device (including no wire bond wall) and line **504** shows the results for the device of FIG. **2**B (including the wire bond wall **50**). As seen in FIG. **5**A, there is a sharp reduction in coupling around the operational frequency (approximately 2 GHz) of the Doherty amplifier. In FIG. **5**B, line **506** shows the results for a conventional device (including no wire bond wall) and line **508** shows the results for the device of FIG. **2**B (including the wire bond wall **50**). As seen in FIG. **5**A, there is a sharp reduction in coupling around the operational frequency (approximately 2 GHz) of the Doherty amplifier. This reduction in coupling, provided by the wire bond wall, enables more efficient operation of the amplifier.

In one implementation, the present disclosure provides a package including a substrate, and a first circuit on the substrate. The first circuit includes a first electrical device, a second electrical device, and a first wire bond array interconnecting the first electrical device and the second electrical device. The package includes a second circuit on the substrate adjacent to the first circuit. The second circuit includes a third electrical device, a fourth electrical device, and a second wire bond array interconnecting the third electrical device and the fourth electrical device. The package includes a wire bond wall including a plurality of wire bonds over the substrate between the first circuit and the second circuit. The wire bond wall is configured to reduce an electromagnetic coupling between the first circuit and the second circuit during an operation of at least one of the first circuit and the second circuit.

In another implementation, the present disclosure provides a Doherty amplifier package. The Doherty amplifier package includes a substrate, a carrier amplifier on the substrate, a peaking amplifier on the substrate adjacent to the carrier amplifier, and a plurality of wire bonds on the substrate. The plurality of wire bonds are interconnected and run along a region of the substrate located between at least a portion of the carrier amplifier and the peaking amplifier. The plurality of wire bonds form a wire bond wall configured to reduce an electromagnetic coupling between the carrier amplifier and the peaking amplifier during an operation of at least one of the carrier amplifier and the peaking amplifier.

In another implementation, the present disclosure provides a method including attaching a carrier amplifier on a substrate, attaching a peaking amplifier on the substrate adjacent to the carrier amplifier, and forming a plurality of interconnected wire bonds on the substrate along a region of the substrate located between at least a portion of the carrier amplifier and the peaking amplifier. The plurality of wire bonds form a wire bond wall configured to reduce an electromagnetic coupling between the carrier amplifier and the peaking amplifier during an operation of at least one of the carrier amplifier and the peaking amplifier.

Although the present disclosure describes specific examples, embodiments, and the like, various modifications and changes can be made without departing from the scope of the present disclosure as set forth in the claims below. For example, although the exemplary methods, devices, and systems described herein are in conjunction with a configuration for the aforementioned device, the skilled artisan will readily recognize that the exemplary methods, devices, and systems may be used in other methods, devices, and systems and may be configured to correspond to such other exemplary methods, devices, and systems as needed. Further, while at least one embodiment has been presented in the foregoing detailed description, many variations exist. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present disclosure. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments are not intended to be construed as a critical, required, or essential feature or element of any or all of the claims.

What is claimed is:

1. A package, comprising:

a substrate;

a first circuit on the substrate, the first circuit including a first electrical device, a second electrical device, and a first wire bond array interconnecting the first electrical device and the second electrical device;

a second circuit on the substrate adjacent to the first circuit, the second circuit including a third electrical device, a fourth electrical device, and a second wire bond array interconnecting the third electrical device and the fourth electrical device;

a plurality of connection pads on the substrate between the first circuit and the second circuit; and

a wire bond wall including a plurality of wire bonds over the substrate between the first circuit and the second circuit and electrically connecting the plurality of connection pads, the wire bond wall being configured to reduce an electromagnetic coupling between the first circuit and the second circuit during an operation of at least one of the first circuit and the second circuit.

2. The package of claim **1**, wherein the plurality of wire bonds are interconnected and run along a region of the substrate that is between at least a portion of the first circuit and the second circuit.

3. The package of claim **1**, wherein the plurality of wire bonds are arranged in at least a first row of wire bonds and a second row of wire bonds and wherein the first row of wire bonds is arranged in parallel with the second row of wire bonds.

4. The package of claim **1**, wherein the first circuit is a carrier amplifier of a Doherty amplifier.

5. The package of claim **4**, wherein the second circuit is a peaking amplifier of the Doherty amplifier.

6. The package of claim **1**, wherein the wire bond wall is connected to a ground voltage terminal.

7. The package of claim **1**, wherein the wire bond wall is connected to an integrated passive device.

8. The package of claim **7**, wherein at least one of a capacitance and an inductance of the integrated passive device is selected to reduce an electromagnetic coupling between the first circuit and the second circuit over a range of frequencies when the integrated passive device is connected to the wire bond wall.

9. The package of claim **1**, wherein at least one of the first electrical device, second electrical device, third electrical device, and fourth electrical device includes at least one of a capacitor, and a transistor.

10. A Doherty amplifier package, comprising:

a substrate;

a carrier amplifier on the substrate;

a peaking amplifier on the substrate adjacent to the carrier amplifier; and

a plurality of wire bonds on the substrate, the plurality of wire bonds being interconnected and running along a region of the substrate located between at least a portion of the carrier amplifier and the peaking amplifier, the plurality of wire bonds forming a wire bond wall configured to reduce an electromagnetic coupling between the carrier amplifier and the peaking amplifier during an operation of at least one of the carrier amplifier and the peaking amplifier.

11. The Doherty amplifier package of claim **10**, including a plurality of connection pads over the substrate and wherein the plurality of wire bonds electrically interconnect the connection pads.

12. The Doherty amplifier package of claim **11**, wherein the plurality of connection pads are connected to a ground voltage.

13. The Doherty amplifier package of claim **10**, wherein the plurality of wire bonds are connected to a ground voltage terminal.

14. The Doherty amplifier package of claim **10**, wherein the plurality of wire bonds are connected to an integrated passive device.

15. The Doherty amplifier package of claim **14**, wherein the integrated passive device has at least one of a capacitance and an inductance selected to reduce an electromagnetic coupling between the carrier amplifier and the peaking amplifier over a range of frequencies when the integrated passive device is connected to the plurality of wire bonds and during an operation of at least one of the carrier amplifier and the peaking amplifier.

16. The Doherty amplifier package of claim **10**, wherein:

the carrier amplifier includes a first wire bond array interconnecting a first electrical device of the carrier amplifier and a second electrical device of the carrier amplifier; and

the peaking amplifier includes a second wire bond array interconnecting a third electrical device of the carrier amplifier and a fourth electrical device of the carrier amplifier.

17. A method, comprising:

attaching a carrier amplifier on a substrate;

attaching a peaking amplifier on the substrate adjacent to the carrier amplifier; and

forming a plurality of interconnected wire bonds on the substrate along a region of the substrate located between at least a portion of the carrier amplifier and the peaking amplifier, the plurality of wire bonds forming a wire bond wall configured to reduce an electromagnetic coupling between the carrier amplifier and the peaking amplifier during an operation of at least one of the carrier amplifier and the peaking amplifier.

18. The method of claim **17**, including forming a plurality of connection pads over the substrate, wherein the plurality of wire bonds electrically interconnect the connection pads.

19. The method of claim **18**, including connecting the plurality of connection pads to a ground voltage terminal.

20. The method of claim **17**, including:

mounting an integrated passive device to the substrate; and

connecting the plurality of wire bonds to the integrated passive device.

21. A package, comprising:

a substrate;

a first circuit on the substrate;

a second circuit on the substrate adjacent to the first circuit;

an electronic component on the substrate between the first circuit and the second circuit;

a first lead on a first side of the package connected to the first circuit;

a second lead on a second side of the package connected to the first circuit, the second side of the package being opposite the first side of the package;

a third lead on the first side of the package connected to the second circuit;

a fourth lead on the second side of the package connected to the second circuit;

a first terminal on the first side of the package between the first lead and the second lead, the first terminal being connected to the electronic component; and

a second terminal on the second side of the package between the third lead and the fourth lead, the second terminal being connected to the electronic component.

22. The package of claim **21**, wherein the electronic component is configured to reduce an electromagnetic coupling between the first circuit and the second circuit during an operation of at least one of the first circuit and the second circuit.

23. The package of claim **22**, wherein the electronic component includes a wire bond wall.

24. The package of claim **23**, including a plurality of connection pads over the substrate and wherein the wire bonds of the wire bond wall electrically interconnect the connection pads.

25. The package of claim **23**, wherein the wire bond wall is connected to an integrated passive device.

26. The package of claim **3**, wherein a first wire bond in the first row of wire bonds is connected to a first connection pad in the plurality of connection pads and none of the wire bonds in the second row of wire bonds are connected to the first connection pad.

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